# UNITED STATES PATENT AND TRADEMARK OFFICE

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| 09/781,803 | 02/12/2001 | Dwight D. Griffin | CM01905G | 8998 |

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| EXAMINER |
|---|
| AUVE, GLENN ALLEN |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2111 | |

DATE MAILED: 03/12/2004

5

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No.<br>09/781,803 | Applicant(s)<br>GRIFFIN ET AL. |
|---|---|---|
| | Examiner<br>Glenn A. Auve | Art Unit<br>2111 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

### Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☒ This action is **FINAL**.     2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

4)☒ Claim(s) *1-7 and 9-28* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

### Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All    b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1.      The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2.      Claims 1-7 and 9-28 are rejected under 35 U.S.C. 102(a) as being anticipated by

applicant's admitted prior art (AAPA).

As per claim 1, AAPA shows an integrated circuit comprising a universal bus

(fig.1,(100)); a CPU (200); and a program control unit (PCU) comprising at least on program

control register (311) coupled to the universal bus for receiving control signals via the universal

bus only (300). AAPA shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. AAPA also shows a plurality of CPUs

coupled to the universal bus (page 1, lines 24-25 of the specification). AAPA shows all of the

elements recited in claim 2.

As for claim 3, the argument for claim 1 applies. AAPA also shows a plurality of

peripheral devices coupled to the universal bus (page 1, lines 24-25 of the specification). AAPA

shows all of the elements recited in claim 3.

As for claim 4, the argument for claim 3 applies. AAPA also shows that the plurality of

peripheral devices are selected from the group consisting of PCUs, ALUs, cyclic redundancy

checkers, data encryption standard engines, data transceivers, secure memory units, memory

mapping units, data registers, data stores, and other memory storage devices (at least in page

1, lines 21-24). AAPA shows all of the elements recited in claim 4.

As for claim 5, the argument for claim 2 applies. AAPA also shows that at least one of the plurality of CPUs controls the bus at any moment in time (inherent in the function of a bus master device CPU). AAPA shows all of the elements recited in claim 5.

As for claim 6, the argument for claim 3 applies. AAPA also shows that the plurality of peripheral devices are slaved to the bus (300,370,390). AAPA shows all of the elements recited in claim 6.

As for claim 7, the argument for claim 1 applies. AAPA also shows that the PCU has at least one instruction set (device 300 operates according to some sort of instruction set which is inherent in the use of such electronic computing devices and the device has a structure similar to that of the CPU 200 which is described in the specification as operating according to an instruction set on pages 3-4) and the CPU has at least one instruction set (pages 3-4). AAPA shows all of the elements recited in claim 7.

As for claim 9, the argument for claim 7 applies. AAPA also shows that the PCU instruction set is stored separately from the CPU's instruction set (at least in figure 1 wherein the device 300 has its own set of instruction registers and control unit). AAPA shows all of the elements recited in claim 9.

As for claim 10, the argument for claim 9 applies. AAPA also shows that the PCU instruction set can be altered without altering the CPU's instruction set (at least in figure 1 wherein the device 300 has its own set of instruction registers and control unit so that the instruction set of that particular device can be altered without regard to any other instruction set). AAPA shows all of the elements recited in claim 10.

As for claim 25, the argument for claim 1 applies. AAPA also shows a memory module (380) coupled to the PCU via a memory bus (372,373,374 and via the memory controller). AAPA shows all of the elements recited in claim 25.

As per claim 11, AAPA shows an application specific integrated circuit comprising a universal bus (fig.1,(100)); a CPU (200); and a program control unit (PCU) comprising at least one program control register (311) coupled to the universal bus for receiving control signals via the universal bus only (300) wherein the CPU is coupled to the PCU without dedicated control lines (fig.1). AAPA shows all of the elements recited in claim 11.

As for claim 12, the argument for claim 11 applies. AAPA also shows a memory mapping unit (370) slaved to the bus for translating logical addresses used by the CPU to physical addresses. AAPA shows all of the elements recited in claim 12.

As for claim 26, the argument for claim 11 applies. AAPA also shows a memory module (380) coupled to the PCU via a memory bus (372,373,374 and via the memory controller). AAPA shows all of the elements recited in claim 26.

As for claim 13, the argument for claim 11 applies. AAPA also shows that the CPU communicates with the PCU by way of the universal bus only (fig.1). AAPA shows all of the elements recited in claim 13.

As per claim 14, AAPA shows a microcontroller comprising a universal bus having physical address lines (fig.1,(100)); a CPU having an instruction set and employing logical addressing (200); and a program control unit (PCU) having an instruction set and comprising at least one program control register (311) and coupled to the universal bus for receiving control signals via the universal bus only (300) wherein the CPU is coupled to the PCU without dedicated control lines (fig.1). AAPA shows all of the elements recited in claim 14.

As for claim 15, the argument for claim 14 applies. AAPA also shows that the PCU instruction set is stored separately from the CPU's instruction set (at least in figure 1 wherein the device 300 has its own set of instruction registers and control unit). AAPA shows all of the elements recited in claim 15.

As for claim 16, the argument for claim 14 applies. AAPA also shows that the PCU instruction set can be altered without altering the CPU's instruction set (at least in figure 1 wherein the device 300 has its own set of instruction registers and control unit so that the instruction set of that particular device can be altered without regard to any other instruction set). AAPA shows all of the elements recited in claim 16.

As for claim 27, the argument for claim 14 applies. AAPA also shows a memory module (380) coupled to the PCU via a memory bus (372,373,374 and via the memory controller). AAPA shows all of the elements recited in claim 27.

As per claim 17, AAPA shows an application specific computing device having integrated circuit comprising a universal bus (fig.1,(100)); a CPU (200); and a program control unit (PCU) comprising at least one program control register (311) coupled to the universal bus for receiving control signals via the universal bus only (300). AAPA shows all of the elements recited in claim 17.

As for claim 18, the argument for claim 17 applies. AAPA also shows that the PCU has an instruction set and the CPU has an instruction set, the PCU instruction set being stored and maintained separately from the CPU instruction set (at least in figure 1 wherein the device 300 has its own set of instruction registers and control unit). AAPA shows all of the elements recited in claim 18.

As for claim 19, the argument for claim 18 applies. AAPA also shows that the PCU instruction set can be altered without altering the CPU's instruction set (at least in figure 1 wherein the device 300 has its own set of instruction registers and control unit so that the instruction set of that particular device can be altered without regard to any other instruction set). AAPA shows all of the elements recited in claim 19.

As for claim 20, the argument for claim 17 applies. AAPA also shows that the CPU is coupled to the PCU without dedicated control lines (fig.1). AAPA shows all of the elements recited in claim 20.

As for claim 21, the argument for claim 17 applies. AAPA also shows a plurality of CPUs coupled to the universal bus (page 1, lines 24-25 of the specification). AAPA shows all of the elements recited in claim 21.

As for claim 22, the argument for claim 17 applies. AAPA also shows a plurality of peripheral devices coupled to the universal bus (page 1, lines 24-25 of the specification). AAPA shows all of the elements recited in claim 22.

As for claim 23, the argument for claim 17 applies. AAPA also shows the device being selected from the group of devices consisting of smartcards, calculators, personal organizers, personal communicators, consumer electronic devices, home and office equipment/appliances, readers/scanners, wireless control units, and combinations thereof (page 1, lines 10-14). AAPA shows all of the elements recited in claim 23.

As for claim 28, the argument for claim 17 applies. AAPA also shows a memory module (380) coupled to the PCU via a memory bus (372,373,374 and via the memory controller). AAPA shows all of the elements recited in claim 28.

As per claim 24, AAPA shows an integrated circuit comprising a universal bus having physical address lines with associated physical addresses(fig.1,(100)); a CPU (200); and a program control unit (PCU) comprising at least one program control register (311) coupled to the universal bus (300) and a memory mapping unit (370) slaved to the bus for translating logical addresses used by the CPU to physical addresses. AAPA shows all of the elements recited in claim 24.

### R sponse to Arguments

3.      Applicant's arguments filed January 20, 2004, have been fully considered but they are

not persuasive. With respect to the rejection under 35 USC 102(a) applicant alleges that the

phrase "at least one program address register" has been added to the PCU limitation. However

this is not correct. Applicant has added the phrase "at least one program _control_ register" to the

claims. Such a register is shown by reference numeral 311. Therefore this argument is not

persuasive.

### Conclusion

4.      **THIS ACTION IS MADE FINAL.**  Applicant is reminded of the extension of time policy as

set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action.  In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action.  In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date

of this final action.

5.      Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Glenn A. Auve whose telephone number is (703) 305-9638.  The

examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
March 9, 2004